L Number	Hits	Search Text	DB	Time stamp
4	2	(integrated adj circuit $5processor $5controller cpu) with loop same hardware same (model$ simulat$ emulat$) and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/28 10:39
14	0	(integrated adj circuit $5processor $5controller) with idle near loop and hardware same (model$ simulat$ emulat$) and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/28 11:04
15	0	(integrated adj circuit $5processor $5controller) same idle near loop and hardware same (model$ simulat$ emulat$) and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/28 11:04
16	4	(integrated adj circuit $5processor $5controller) and (idle endless) near loop and hardware same (model$ simulat$ emulat$) and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/28 11:05
17	1	(integrated adj circuit $5processor $5controller) same hardware same (model$ simulat$ emulat$) and (idle endless) near loop and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/28 11:05
18	15	716/4 and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/28 11:20
19	11	716/5 and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/28 11:20
22	0	716/$ and (integrated adj circuit microprocessor microcontroller) and (bus near model$) with hardware and (disabl$ inactive) near3 processor and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/28 11:21
23	0	716/4 and (integrated adj circuit $5processor $5controller) near3 loop same hardware same (model$ simulat$ emulat$) and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/28 11:21
24	0	716/5 and (integrated adj circuit $5processor $5controller) near3 loop same hardware same (model$ simulat$ emulat$) and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/28 11:22

25	0	716/6 and (integrated adj circuit $5processor $5controller) near3 loop same hardware same (model$ simulat$ emulat$) and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/28 11:22
26	0	716/$ and (integrated adj circuit $5processor $5controller) near3 loop same hardware same (model$ simulat$ emulat$) and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/28 11:22
20	10	716/6 and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/28 11:27